2811

503.377.0100

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): M. OGINO

Serial No.: 09/429,297

Filed: October 28, 1999

For: SEMICONDUCTOR DEVICE, SEMICONDUCTOR WAFER, SEMICONDUCTOR MODULE, AND A METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE

Group: 2811

Examiner:

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

March 31, 2000

Sir:

The following preliminary amendments and remarks are respectfully submitted in connection with the above-identified application.

IN THE CLAIMS

Please amend the claims as follows:

Claim 1, line 2, before "semiconductor" insert --a--, same line 2, delete "chips" and insert --chip--.

Claim 2, line 2, before "semiconductor" insert --a--, same line 2, delete "chips" and insert --chip--.

Claim 3, line 2, before "semiconductor" insert --a--, same line 2, delete "chips" and insert --chip--;

line 14, delete ",".

Claim 4, line 1, delete "claims";

line 2, delete "from".

Claim 9, line 2, before "semiconductor" insert --a--, same line 2, delete "chips" and insert --chip--.

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10. (Amended) A semiconductor wafer comprising:

a chip having a plurality of chip areas comprising circuits and electrodes, respectively,

a stress relaxing layer provided on a plane of said chip, whereon the circuits and the electrodes [of said chip area] are formed,

a circuit layer provided on said stress relaxing layer, and connected to said electrodes, and

external terminals provided on said circuit layer, wherein

an organic protecting film is provided on the plane opposite to the plane, whereon said stress relaxing layer is provided, of said chip [areas].

11. (Amended) A semiconductor wafer comprising:

a chip having a plurality of chip areas comprising circuits and electrodes, respectively,

a porous stress relaxing layer provided on a plane of said chip, whereon the circuits and the electrodes of said chip area are formed,

a circuit layer provided on said stress relaxing layer,

via-holes provided between said electrodes and said circuit layer,

conductive portions for electrically connecting [electrically] said circuit layer and said electrodes in said via-holes,

external terminals provided at designated portions on said circuits in a grid array pattern, and

an organic protecting film provided on the plane opposite to the stress relaxing layer of said [area].

Claim 12, line 1, after "any" insert --one--.

Claim 13, line 1, after "any" insert --one--.

17. (Amended) A semiconductor wafer comprising:

a chip having a plurality of chip areas comprising circuits and electrodes, respectively,

a porous stress relaxing layer provided on a plane of said chip, whereon the circuits and the electrodes of said chip area are formed,

a circuit layer provided on said stress relaxing layer,

anisotropic conductive material for connecting electrically [said] electrodes on [said] a chip are and [said] a circuit layer,

external terminals provided at designated portions on said circuits in a grid array pattern, and

an organic protecting film provided on the plane

opposite to the plane, wherein said circuits and electrodes are formed, of said chip [area].

18. (Amended) A method [for] of manufacturing a semiconductor device comprising the steps of:

forming a stress relaxing layer on a plane, whereon circuits and electrodes of respective chip areas are formed, of a semiconductor wafer,

forming an organic protecting film on the plane of said semiconductor wafer opposite to the plane[,] where the electrodes of said respective chip areas are formed,

forming via-holes in said stress relaxing layer on said chip areas,

forming conductive portions in said via-holes,

forming circuits on said stress relaxing layer,

forming external terminals on said circuit layer, and

cutting said chip areas, the substrate comprising said circuits, and said organic protecting film along a same plane so that [the] a semiconductor device obtained by the cutting becomes a minimum operation unit.

Claim 19, line 1, delete "for" and insert --of--, same line 1, after "manufacturing" insert --a--;

line 3, after "forming" insert --a--;

line 8, delete "to" and inset --on--;

line 15, delete "the" (first occurrence) and insert --a--.

Claim 20, line 2, delete "from".

IN THE ABSTRACT

Please amend the abstract as follows:

Line 3, delete ":" and insert --,--, same line 3, after "wherein" insert --:--;

Line 4, delete "damages" and insert --damage--, same line 4, after "at" insert --the--;

Line 5, after "cracks" insert --occurring--;

Line 7, after "producibility." insert --The semiconductor includes a--;

Line 8, delete in its entirety;

Line 18, delete "a" and insert --the--.

REMARKS

The specification and abstract of the disclosure have been amended to correct errors of a typographical and grammatical nature. Due to the excessive corrections thereto, applicants submit herewith a Substitute Specification, along with a marked-copy of the original specification for the Examiner's convenience. Applicants submit that the substitute specification includes no new matter. Therefore, entry of the Substitution Specification is respectfully requested.

The claims have also been amended to more clearly describe the features of the present invention.

Also submitted herewith is a proposed amendment to the drawings, wherein Figs. 1, 3-7 and 11 have been amended at

this time. Upon receipt of the approval of the amendment to the drawings and receipt of a Notice of Allowance, the proposed drawing corrections will be effected in accordance with present practice.

Entry of the preliminary amendments and examination of the application is respectfully requested.

To the extent necessary, Applicants petition for an extension of time under 37 CFR § 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Deposit Account No. 01-2135 (Case No. 503.37770X00) and please credit any excess fees to such Deposit Account.

Respectfully submitted,

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